Patent claims

1. A method for the production of a bipolar transistor comprising a highly doped extrinsic base (EB),
- in which a base layer (BS) is provided on a semiconductor substrate (HLS),
- in which a dielectric layer (DS) is deposited in weakly doped or undoped fashion on the base layer,
- in which a dopant of the first conductivity type is introduced into the dielectric layer,
- in which, in a controlled thermal step, the dopant indiffuses into the semiconductor substrate from the dielectric layer, an extrinsic base doped in low-resistance fashion arising.

2. The method as claimed in claim 1,
in which an oxide layer is deposited as the dielectric layer (DS), BF_2 subsequently being introduced into said oxide layer as the dopant.

3. The method as claimed in claim 1 or 2,
in which an emitter window (EF) is opened in the dielectric layer (DS).

4. The method as claimed in one of claims 1 to 3,
in which an implantation mask is applied and patterned in such a way that an opening remains in a region provided for the later extrinsic base (EB).

5. The method as claimed in claim 3 or 4,
in which, before the dopant is introduced into the dielectric layer (DS), the emitter (E) is produced by application and patterning of a polycrystalline emitter layer doped with a dopant of the second conductivity type above the emitter window (EF).

6. The method as claimed in claim 5,

in which the emitter layer is patterned by means of a photopatterned resist mask that remains on the emitter (E) and is later used as an implantation mask for the implantation of the dopant into the dielectric layer.

7. The method as claimed in one of claims 1 to 6, in which, for the production of the semiconductor substrate (HLS), in a semiconductor wafer (HLW) doped with a dopant of the second conductivity type, active transistor regions (TB) are defined and are electrically insulated by oxide regions (OB), and

- in which a base layer (BS) weakly doped with a dopant of the first conductivity type is grown epitaxially over the whole area.

8. The method as claimed in one of claims 1 to 7, in which a buried collector layer (VK) doped with a dopant of the second conductivity type is produced by implantation in the semiconductor wafer (HLW) in the active transistor region (TB), said collector layer serving for electrical connection of the collector.

9. The method as claimed in one of claims 1 - 8, in which BF_2 is implanted for the introduction of the dopant into the dielectric layer (DS).

10. The method as claimed in one of claims 1 - 8, in which BF_2 can be indiffused into the dielectric layer (DS) from the gas phase.

11. The method as claimed in one of claims 4 - 9, in which the emitter layer is doped with arsenic, in which, during the indiffusion of the dopant into the base layer (BS), arsenic also indiffuses into a surface region of the base layer (BS) from the emitter (E).

12. The method as claimed in one of claims 4 - 10,

in which the dielectric layer (DS) is removed after the patterning of the emitter layer and after the outdiffusion of the dopant in uncovered regions by etching.

13. The method as claimed in one of claims 1 - 11,
- in which an n-doped semiconductor wafer (HLW) is provided,
- in which a p-doped base layer (BS) is grown epitaxially on the semiconductor wafer over the whole area,
- in which a dielectric layer (DS) is applied in weakly doped or undoped fashion on the base layer,
- in which an emitter window (EF) is opened in the dielectric layer,
- the emitter (E) is produced by application and patterning of an As-doped polycrystalline emitter layer above the emitter window,
- in which BF_2 is introduced as the dopant into the dielectric layer with the aid of an implantation mask,
- in which, in a controlled thermal step, boron can be indiffused from the dielectric layer into the base layer in the region of the extrinsic base (EB), the latter acquiring low resistance, and arsenic simultaneously indiffuses into an upper region of the base layer (BS) from the emitter through the emitter window.

14. The method as claimed in claim 13,
in which a photomask applied over an oxide layer over the emitter (E) is used as the implantation mask, said photomask already having been used beforehand for the patterning of the emitter layer.

15. The method as claimed in claim 13 or 14,
in which the collector connection is effected via an n^+-doped buried layer, and in which, over the emitter and in the region of the extrinsic base, the respective

semiconductor is uncovered and metallic contacts are produced above the latter.